Mitesh Khadgi

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Career Objective

To continue to grow in leadership and knowledge, excel in innovative technology and application, interact and share with team members and develop world class solutions to real world challenges.

Educational Qualification

Program	Institution	%/CGPA	Year
Masters : Computer Engineering	University of Texas at Dallas, Richardson	1st Semester	2020 (Expected)
B.Tech : Electrical Engineering **M.Tech** : Microelectronics & VLSI Design	Indian Institute of Technology, Madras	6.35/10	2011
XII, CBSE	B.S.P. Senior Secondary School, Bhilai	66.8	2005
X, CBSE	B.S.P. Senior Secondary School, Bhilai	76.8	2003

Current Semester Courses: Computer Architecture, Design Automation of VLSI Systems

Academic Projects

- Gem5 Branch Prediction, Richardson, UTD, USA — Period: Semester 1
  - Language: C, Perl, Shell Scripting
  - Setup of SPEC CPU2006 benchmarks for L1, L2 cache miss rate & misses calculations
  - Simulation of 2-bit local, bimode, tournament branch predictors
  - Benchmarks used for simulation: 401.bzip2, 429.mcf, 456.hmmer, 458.sjeng, 470.lbm
- Fiduccia-Mattheyses Algorithm implementation, Richardson, UTD, USA — Period: Semester 1
  - Language: C++, Perl
  - Parsing of millions of nodes/nets (circuit-based) in a netlist in seconds
  - Develop a data structure to extract and store the information from netlists
  - Access and Update the data structure with least order of complexity
  - Finding the final optimal cutset depending on 45%-55% area distribution with bi-partitioning algorithm
- Center for Computer Science Education & Outreach — Period: Semester 1
  - Deep Learning with TensorFlow Workshop organized by Prof. Anurag Nagar
  - Big Data Workshop organized by Prof. Jey Veerasamy

Technical Skills

- Software/Hardware Programming Languages: C/C++, Java, Python, CSS, HTML, Verilog, System Verilog, PHP
- Operating Systems: Unix/Linux, Windows
- Hardware tools: Questasim, Xilinx ISE Design Suite, Altera Quartus, Modelsim, Orcad
- Software tools: Visual Studio, Netbeans,, Matlab, Simulink
- Hardware development boards: Altera Cyclone II, Arduino, Spartan II, Spartan 3, Spartan 3E, Virtex 6
- Expertise in Simulation/Synthesis/Verification Methodology: UVM, RTL Design, FPGA Simulation/Synthesis

Professional Experience

- Senior Verification Engineer, SmartSOC Solutions Pvt. Ltd., Bangalore, Karnataka, India (14th August 2017 – 11th May 2018) — Period: 9.5 months
  - SOC Verification (Intel Corporation - Client) Period: 4.5 months
    - Tested GNSS memory accesses using JTAG Protocol
  - IP Verification (Canon India Pvt. Ltd. - Client) Period: 3.5 months
    - Developed 200+ testcases to verify design RTL
    - Tested and debug design RTL integrated with Cadence VIP slave for AXI3/AXI4
    - Generated code coverage results for AXI3/AXI4 testcases
    - Regression testing for around 300+ testcases and 10 different AXI3/AXI4 configurations
- Digital Design Engineer, Asiczen Technologies, Bhubaneshwar, Orissa, India (23rd February 2017 – 8th June 2017) — Period: 3 months
  - AXI4 UVC development
    - Designed an AXI Master UVC using System Verilog, UVM
    - Created a feature list from specification, coverage plan, scoreboard, testcases
    - Tested it with already available AXI Slave UVC
- Design Engineer, iMSpired Pvt. Ltd., Bangalore, India (6th July 2015 – 31st March 2016) — Period: 9 months
  - System Verilog, Universal Verification Methodology (UVM) training
  - Design a Graphical User Interface (GUI) for automated code generation using Java for Assertion/Functional coverage
  - APB Protocol implementation with driver, monitor, scoreboard in UVM environment
  - Priority based arbiter switch RTL design/implementation in Verilog

- Waverin Parser (Bug tracking system) implementation and feature development (Client: Intel Corporation)

- Software Engineer, Design Methodology and Flow Development Team, Intel Mobile Communications, Bangalore, India (7th July 2011 – 31st October 2013) Period: 2 years 4 months
  - Memory Controller Design and Verification with Setup installation for Hybrid-Virtual Prototype enablement across country site locations with AresPeak (Virtex-6 FPGA) emulation board for memory controller IPs
  - Design a methodology for efficient code-generation in Verilog/VHDL, SystemC, C/C++
    - Database management using Clearcase and UTP tracking system
    - Contributed in 4 quarterly release version with old/new feature developments
    - Extensively worked on writing Python generators
- IEEE Volunteer Guide/Mentor at REVA Institute of Technology & Management, Bangalore, India (30th January 2013-February 2015) Period: 2 years 1 month
  - Connecting Cube, an initiative to develop an incubation center where students can bring their ideas to life
  - Mentored and directed students at every step to make their ideas alive with appropriate advices/suggestions
  - Coordination of a group of 7 students for final year projects in Very Large Scale Integration (VLSI)
  - Mentored two projects: Fingerprint recognition algorithm and S-Box Architecture in AES-Encryption algorithm
    - Fingerprint Recognition algorithm using MATLAB (FRA)
    - Enhancement of S-Box Architecture (SBA) in AES-Encryption algorithm with Spartan-3 Xilinx FPGA
- IEEE, Consumer Electronics (CE), Executive Committee Member (EXECOM), Bangalore Section, India (24th February 2013-2016) Period: 3 years

Scholastic Achievements

- Among top 1% candidates qualified for National Talent Search Examination (NTSE) 3 stage (2002)
- Presented an innovative idea in NYC Next Idea, an International Business-Plan Competition in Columbia University (2010)
- IEEE Xplore publication: An adaptive-method for velocity estimation using time-to-digital converter in FPT'2011 (2011)
- Submitted a patent idea-concept on RF technology at Intel Corporation (2012)
- Participated in innovative ideas conference in Software Architecture at Intel Corporation (2012)
- Participated in many initiatives for B-plan competitions around the globe (2010-2012)
- Submitted idea in an innovation competition "Eye of the Tiger" at Intel Corporation (2013)

Extra-curricular Activities

- Selection in Football National Sports Organization (NSO) at IIT Madras (2006)
- Volunteer for Quality Management Control (QMC) at Shaastra, a Technical Festival at IIT Madras (2006)
- An Athlete, participated in (4th position) 5km, 9km long-run competition held at IIT Madras (2008)
- Captain of Road Race Dean's Trophy (9km) and Hostel Athletics Team (2008)
- A Football player, won Bronze medal (2008, 2009)
- A Hockey player, won Gold & Bronze medals (2009, 2010)
- Performed stage-show as guitarist and singer at Intel Cultural Festival (2011, 2012)
- Member of IEEE communications technical society (2011-2013)
- An active member/volunteer in Advanced Humanity, IEEE, Bangalore society (2013)
- Performed as a Singer on Independence Day at University of Texas at Dallas (2018)

Social-activities:

- Participation in Youth Ki Awaaz, an online debate platform for the youths (2009)
- An ambassador of TouchTalent, a hunt for the most talented people (2012)
- Make A Difference (MAD): Volunteer for teaching science, conducting various science experiments and, motivating the children towards science subject in under-developed schools (6-months project) (2012)
- Joy of Giving Week (JGW): Volunteer for collection of used goods and toys for donation to under-privileged children (2013)
- President & Founder, Trace Assist for Disabilities (TAD Student Organization), University of Texas at Dallas (2018)

Hobbies and Interests: Guitar, Singing, Sketching, Reading novels, Listening music, Social-networking, Electronic-gadgets, Traveling, Photography